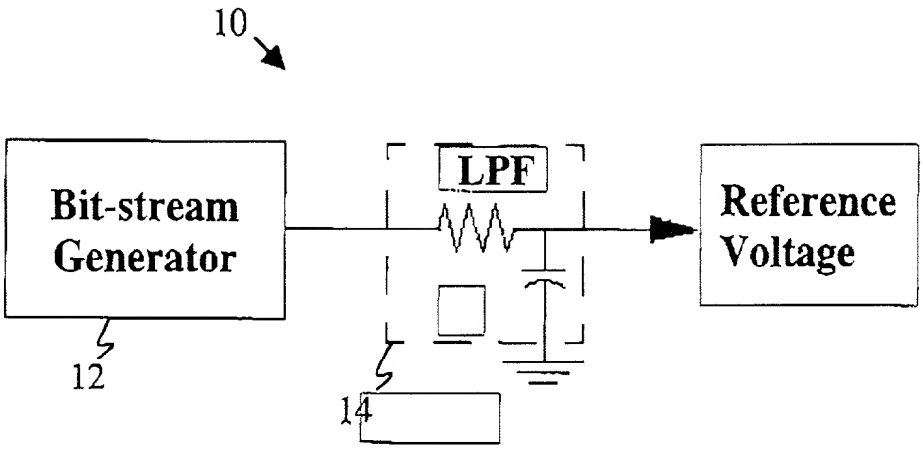
10
Bit-stream Generator
LPF
Reference Voltage
12
14

FIG 1.

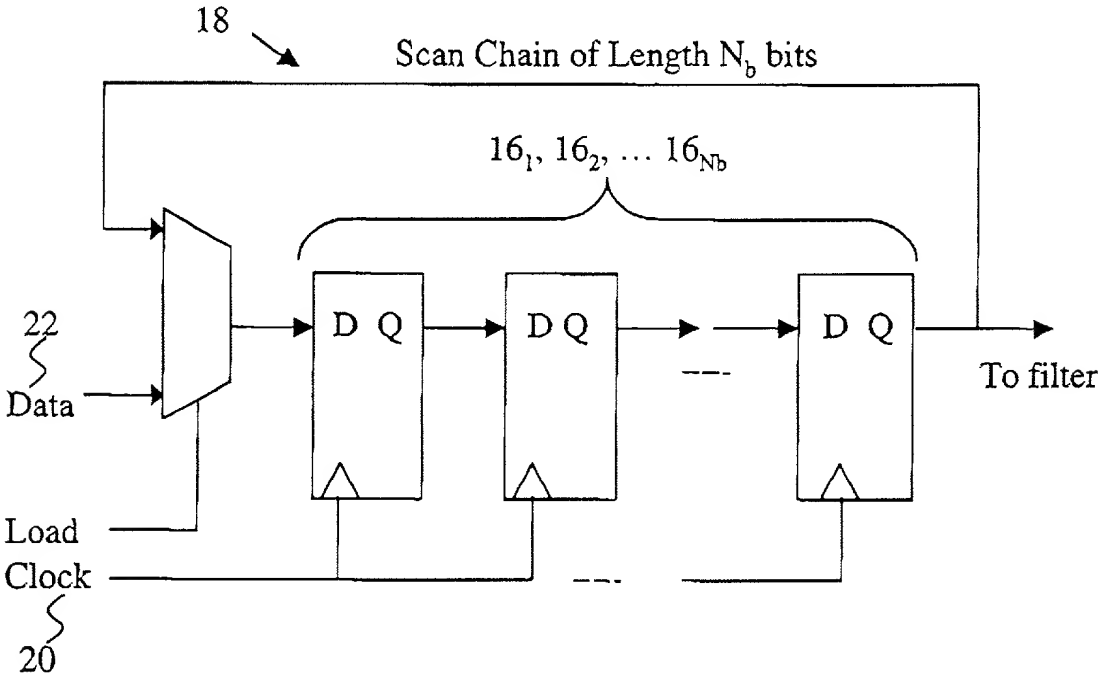
18
Scan Chain of Length N_b bits
16_1, 16_2, ... 16_{Nb}
D Q
D Q
D Q
To filter
22
Data
Load
Clock
20

FIG 2.

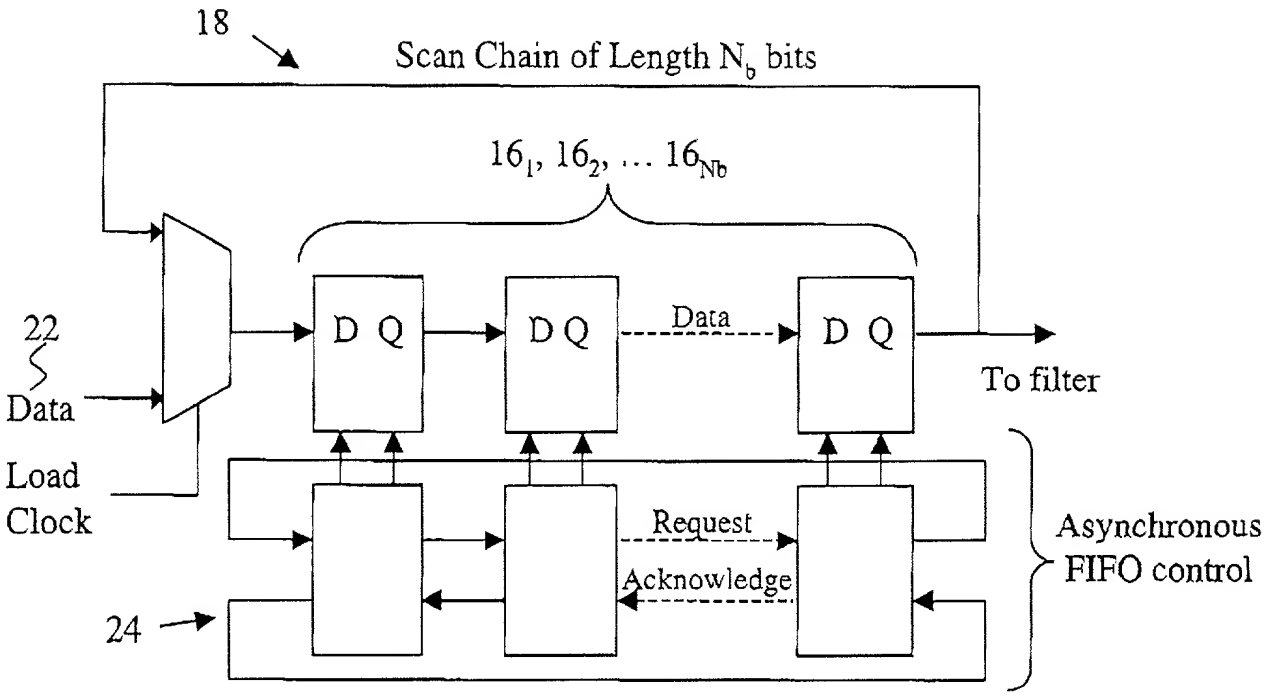
18
Scan Chain of Length N_b bits
16_1, 16_2, ... 16_{Nb}
22
Data
Load
Clock
D Q
D Q
Data
D Q
To filter
Request
Acknowledge
Asynchronous
FIFO control
24

FIG 3.

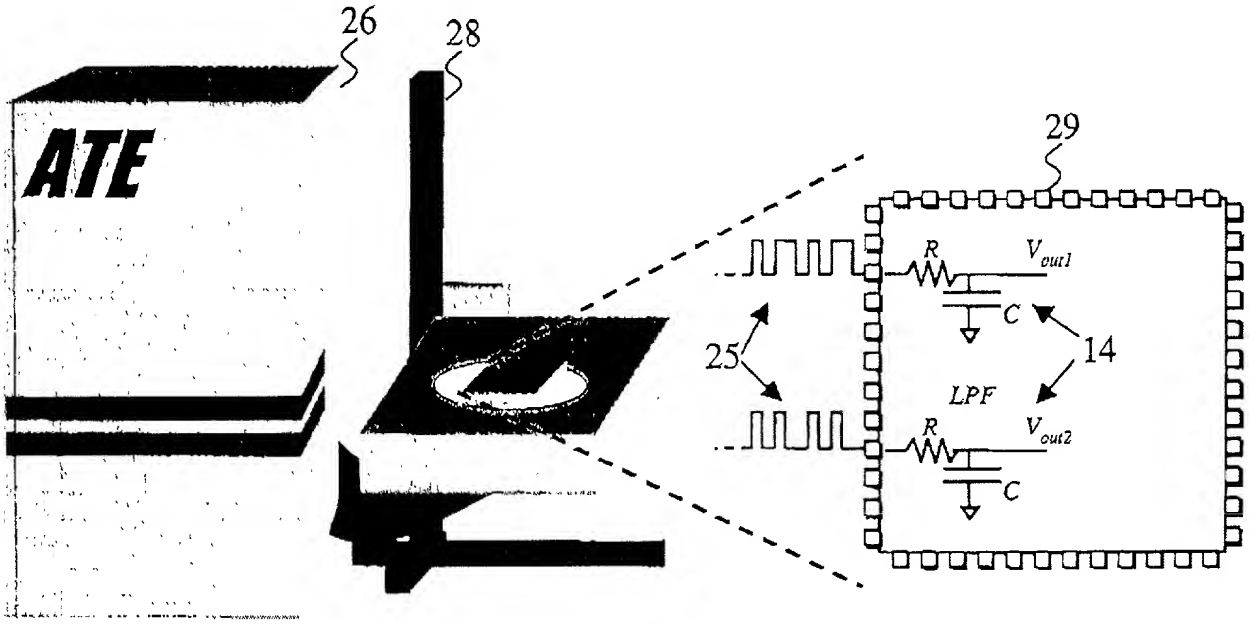
26
28
ATE
29
R
V_{out1}
C
25
14
LPF
R
V_{out2}
C

FIG 4.

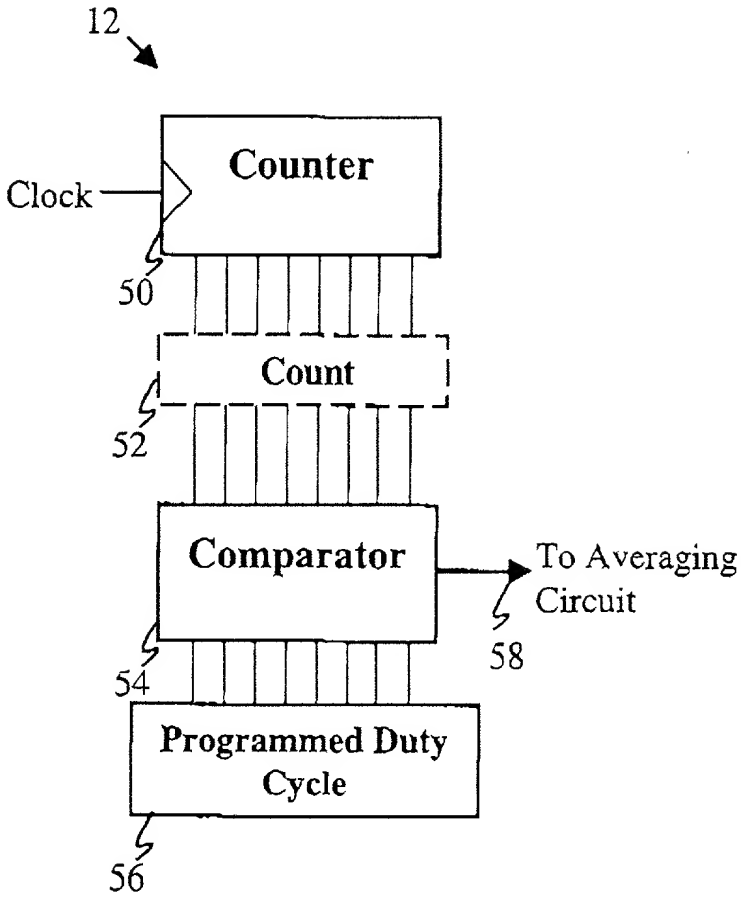
12
Counter
Clock
50
Count
52
Comparator
To Averaging Circuit
58
54
Programmed Duty Cycle
56

FIG 5.

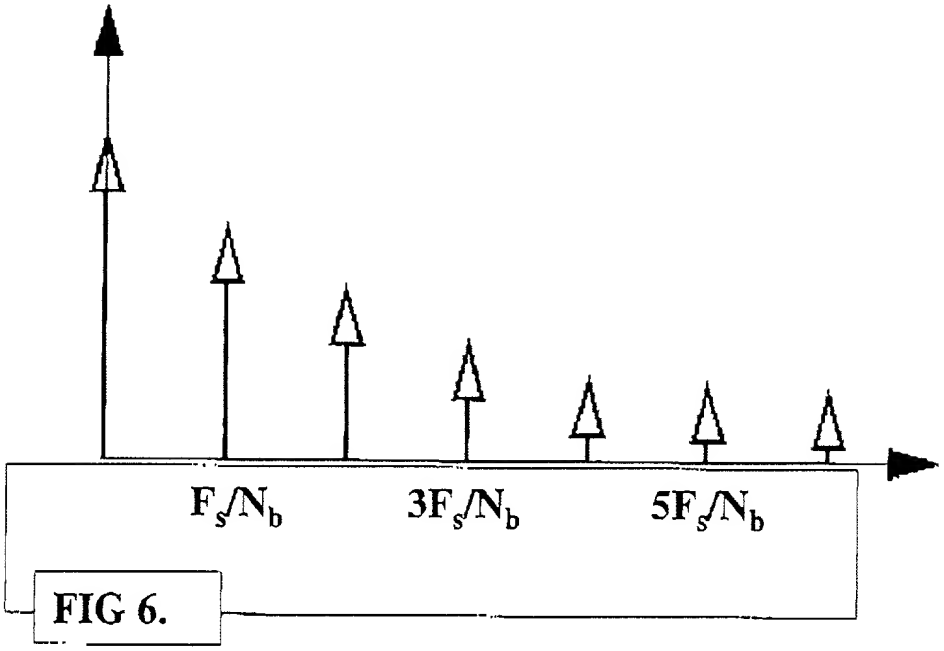
F_s/N_b
$3F_s/N_b$
$5F_s/N_b$

FIG 6.

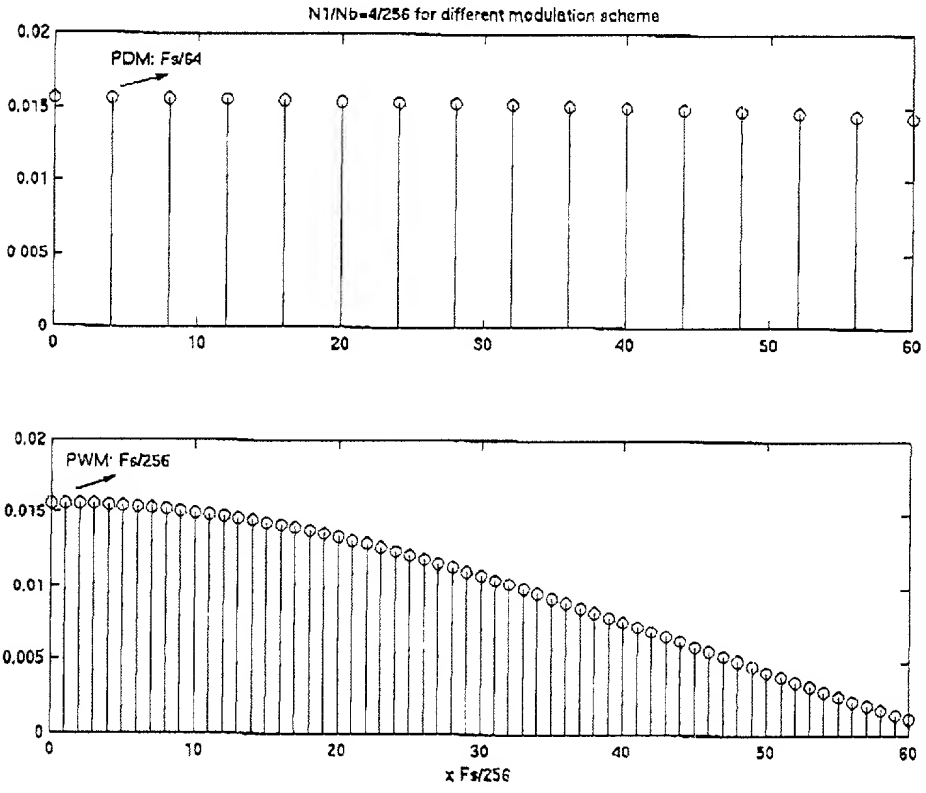
N1/Nb=4/256 for different modulation scheme
PDM: Fs/64
PWM: Fs/256
x Fs/256

FIG 7.

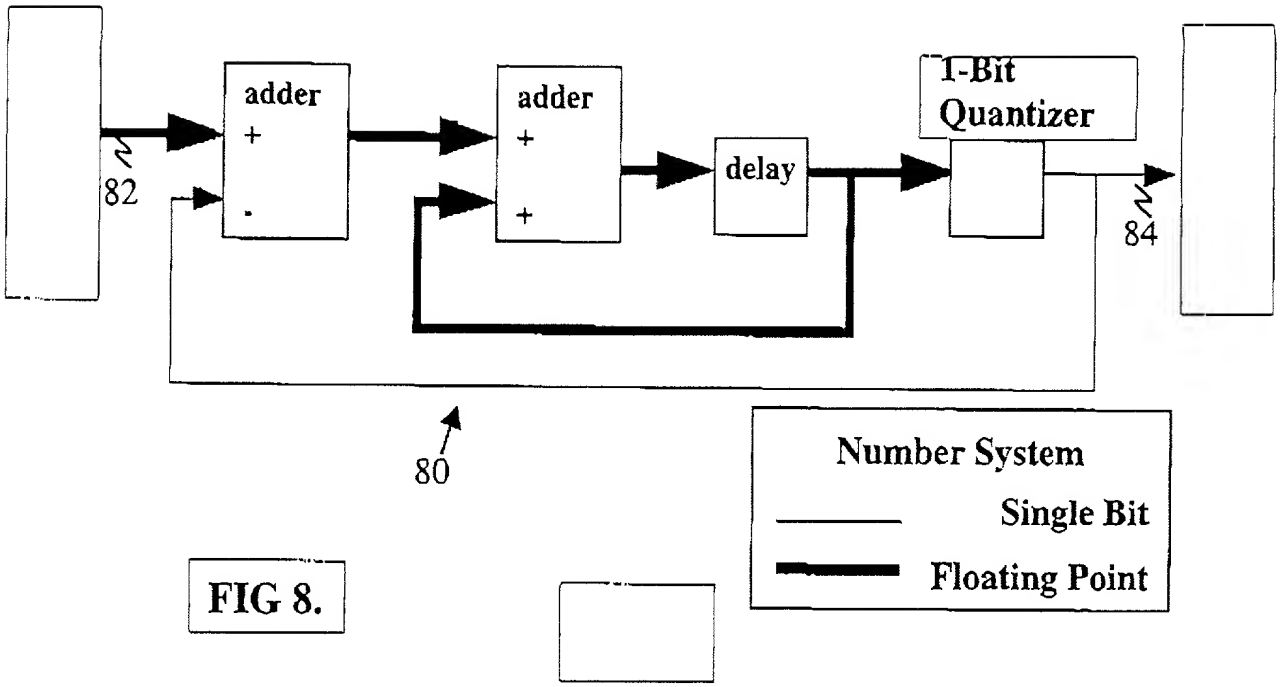
adder
+
-
adder
+
+
delay
1-Bit
Quantizer
82
84
80
Number System
Single Bit
Floating Point

FIG 8.

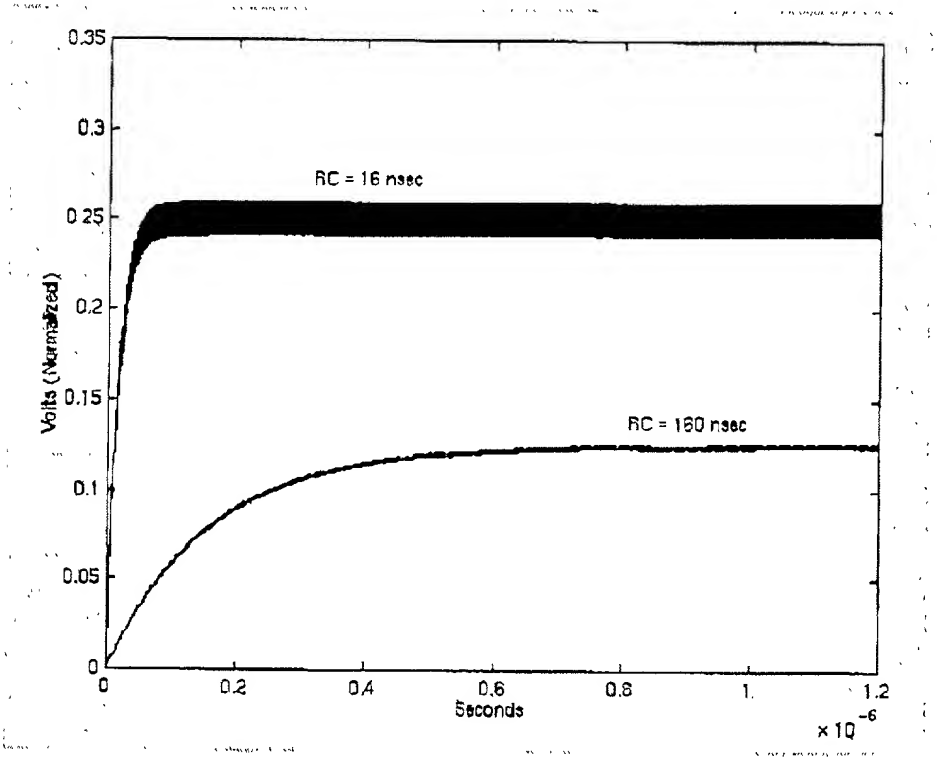
0.35
0.3
0.25
0.2
0.15
0.1
0.05
0
RC = 16 msec
RC = 160 msec
Volts (Normalized)
0
0.2
0.4
0.6
0.8
1.
1.2
Seconds
x 10^-6

FIG 9.

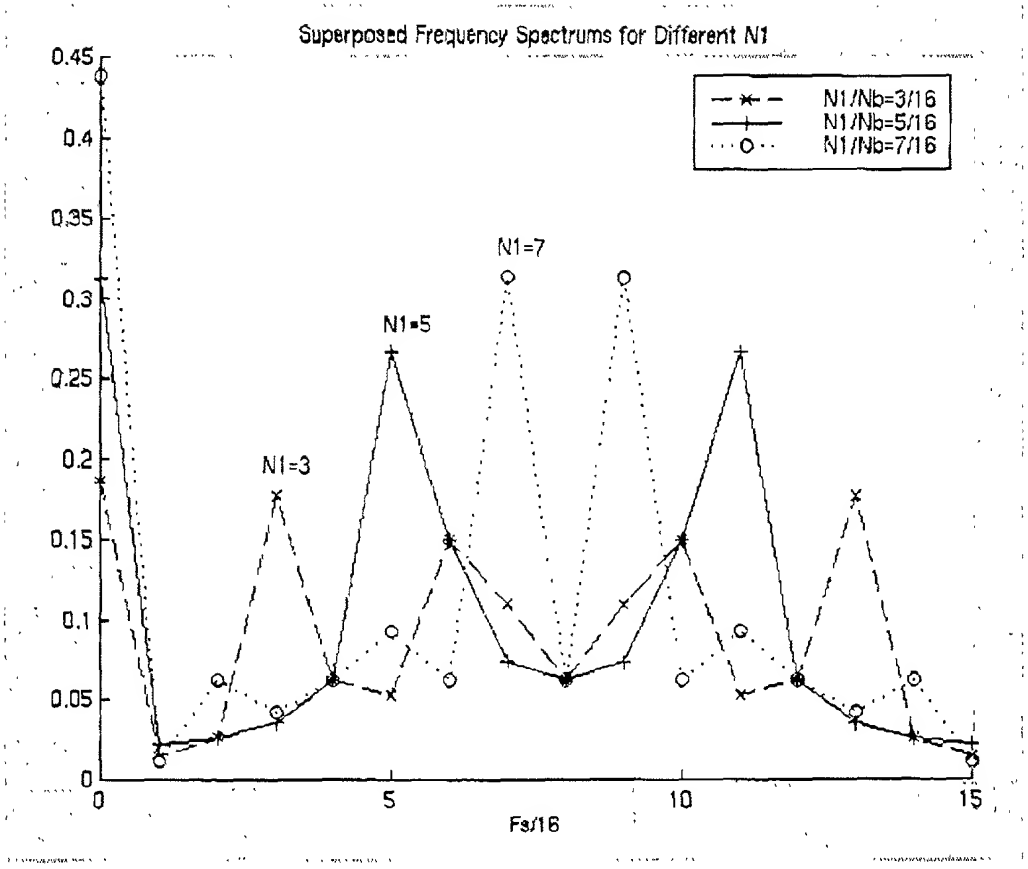
Superposed Frequency Spectrums for Different N1
N1/Nb=3/16
N1/Nb=5/16
N1/Nb=7/16
N1=3
N1=5
N1=7
0.45
0.4
0.35
0.3
0.25
0.2
0.15
0.1
0.05
0
0
5
10
15
Fs/16

FIG 10.

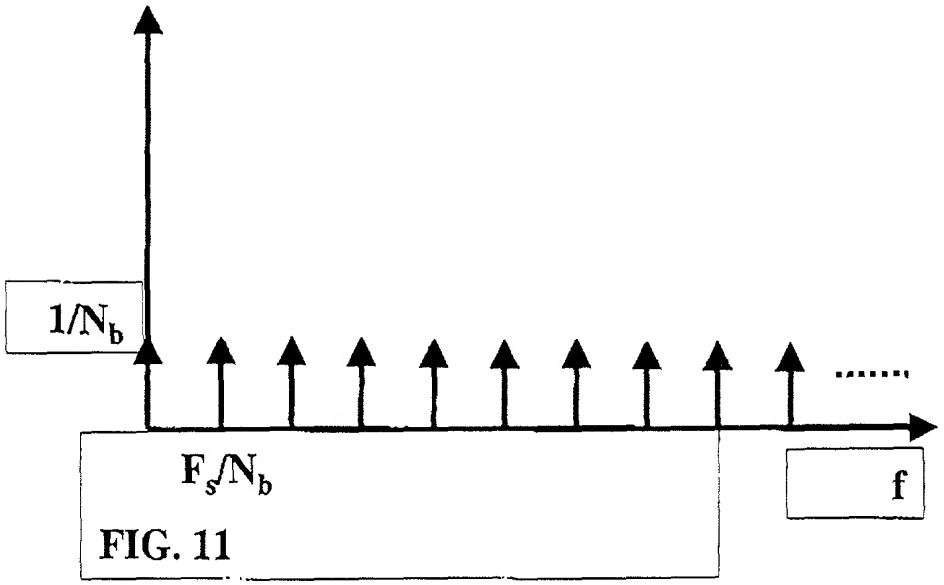
1/Nb
Fs/Nb
f

FIG. 11

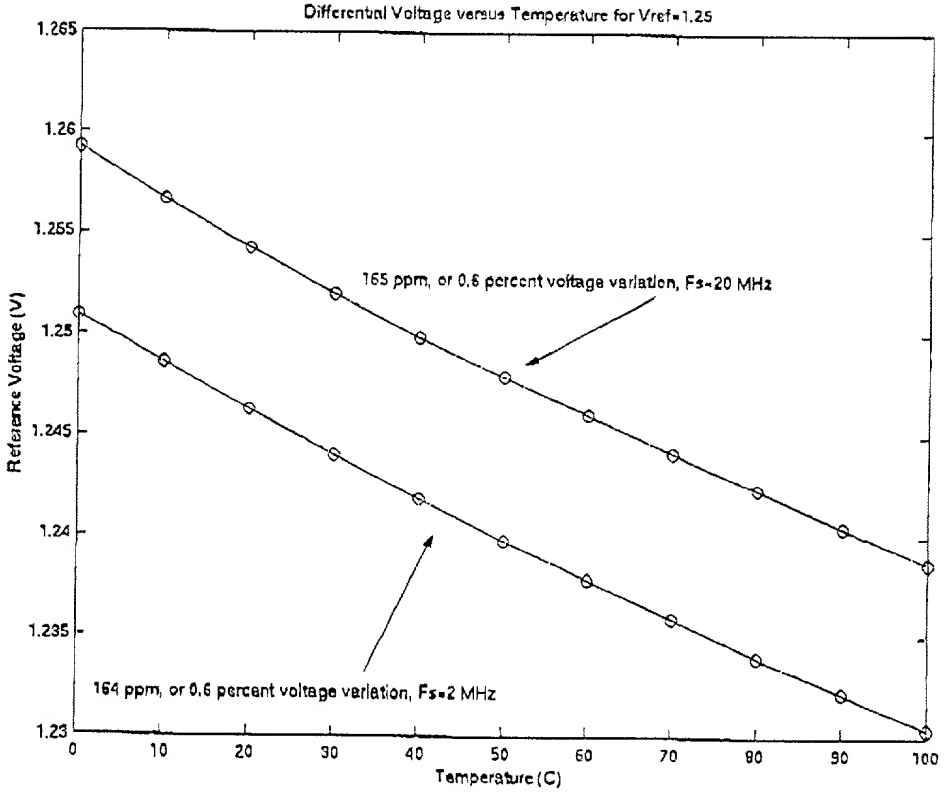
Differential Voltage versus Temperature for Vref=1.25
Reference Voltage (V)
Temperature (C)
165 ppm, or 0.6 percent voltage variation, Fs=20 MHz
164 ppm, or 0.6 percent voltage variation, Fs=2 MHz
1.265
1.26
1.255
1.25
1.245
1.24
1.235
1.23
0
10
20
30
40
50
60
70
80
90
100

FIG 12.

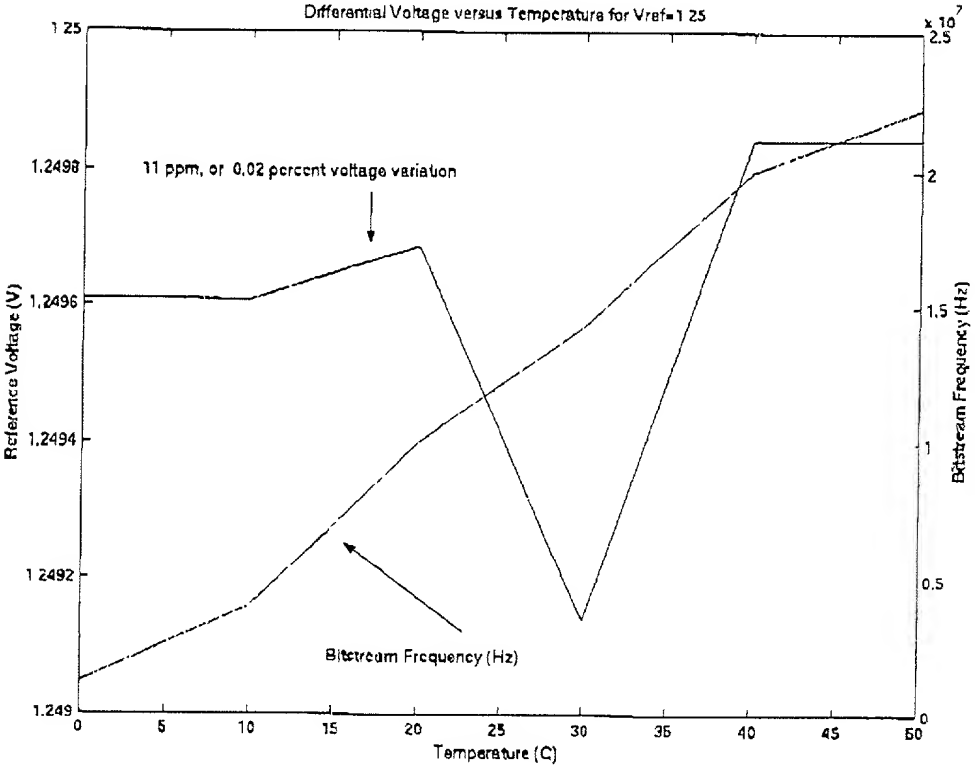
Differential Voltage versus Temperature for Vref=1.25
Reference Voltage (V)
Bitstream Frequency (Hz)
Temperature (C)
11 ppm, or 0.02 percent voltage variation
Bitstream Frequency (Hz)
x 10^7
1.25
1.2498
1.2496
1.2494
1.2492
1.249
2.5
2
1.5
1
0.5
0
0
5
10
15
20
25
30
35
40
45
50

FIG 13.